UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/082,517	02/22/2002	Reno L. Sanchez	X-998 US	5981

24309   7590   09/08/2003

XILINX, INC
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EXAMINER
DIMYAN, MAGID Y

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 09/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

-- *The MAILING DATE of this communication appears on the cover she t with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *16 September 2002* .

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-37* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-37* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on *22 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

    If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____ .

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
      application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

    a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .

4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: .

DETAILED ACTION

Acknowledgement

1.   Receipt is acknowledged of the Preliminary Amendment filed September 16, 2002. It is also acknowledged that the Applicants have amended claims 11 and 21, and added claims 29 – 27. Three of the additional claims are independent claims.

Claim Rejections - 35 USC § 102

2.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3.   Claims 1 – 37 are rejected under 35 U.S.C. 102b as being anticipated by U.S. Patent No. 6,182,247 to Herrmann et al (hereinafter, Herrmann).

4.   Referring to claim 1, Herrmann discloses a technique for embedding a logic analyzer in a programmable logic device (i.e., FPGA-based SoC – see column 1, line 50 to column 2, line 4) that allows debugging of the device in its operating condition (i.e., developing and verifying). Furthermore, all the limitations of the claim of (a) executing

software code for the embedded logic analyzer; (b) defining monitor probe points within

the device; and (c) collecting information from the probe points to facilitate the analysis,

are cited in the invention. See Figs. 3A, 3B, 6; Summary of the Invention (columns 3 -

5).

5.   As per claims 2, 3 and 4, see (4) above as well as column 11, lines 40 – 60,

which cite how to capture data, trace information, and trigger information from the probe

points, as claimed herein.

6.   As per claim 5, see (4) above as well as Fig. 5, which teach the same invention

as claimed herein, of receiving and collecting information via an external tool interfaced

to the embedded logic analyzer (in this case, a computer).

7.   Referring to claims 6 and 7, see above, as well as column 9, line 44 to column

11, line 60, which recite how the waveforms, as claimed herein, are captured.

8.   As per claim 8, see above, as well as column 14, lines 27 – 48, which cite how to

monitor internal nodes as well as a device pin.

9.   Referring to claims 9 and 10, see (4) above, as well as Figs. 3A, 3B; column 9,

lines 44 – 65, which disclose how to program the embedded logic analyzer, as claimed.

10. Claims 11 – 20 contain the same limitations as claims 1 – 10, respectively, and thus the same rejections apply.

11. As per claims 21 and 22, see above; Figs. 3A, 5 and 6; which disclose how the software for the embedded logic analyzer can be can be created by compiling the circuit during customization (i.e., creating a software core), and also shows how an interface and communications port between the logic analyzer and a computer system (external monitor tool) is established and controlled, as claimed.

12. Referring to claim 23, see (11) above; column 10, lines 14 – 24; column 11, lines 51 – 60, which recite how a graphical user interface (GUI) is used to display a signal (waveform) as claimed.

13. As per claim 24, see Fig. 7; column 42 to column 18, line 50, which show the embedded processor system (computer system), used in the invention, as claimed.

14. As per claims 25 – 28, see above; column 10, lines 1 – 67, which teach the use of a GUI, in accordance with inventions cited in the claims.

15. Referring to claim 29, 30 and 31 see (4) above; column 1, lines 45 – 50; Fig. 7; column 17, line 43 to column 18, line 50, which recite the computer system that contains a processor, and the same limitations of claim1.

16.   As per claim 32, see (4) and (15) above, which contain the same limitations, and

thus the same rejections apply.

17.   As per claims 33 and 34, see (15) above which contains the same limitations.

18.   Referring to claims 35 – 37, see (4), (5), and (12) above which contain the same

limitations of the FPGA-based IC development and verification system with a GUI

interface as claimed herein.

Conclusion

19.   The prior art made of record and not relied upon is considered pertinent to

applicant's disclosure.

Pub. No. US 2003/0097615 to Corti et al cites an on-chip logic analysis (OCLA) system

that captures data processed by a signal processing logic core embedded in a single

SoC device without interrupting operations of the signal processing logic core.

Pub. No. US 2002/0037477 to Veenstra et al discloses an enhanced logic analyzer

embedded in a programmable logic device that allows signals to be captured both

before and after a trigger condition, and stores the logic signals for viewing on a computer.

U.S. Patent No. 6,564,347 to Mates teaches a method and apparatus for testing an IC using an on-chip programmable logic analyzer unit embedded in the IC to test a function of the circuit.

U.S. Patent No. 6,442,725 to Schipke et al describes a system and method for providing intelligence to an analysis probe being utilized by logic analyzers.

Pub. No. US 2003/0110453 to Bailis et al recites a method and system for use of a field programmable function within a chip to enable configurable I/O signal timing characteristics.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Magid Y Dimyan whose telephone number is (703) 308-1354. The examiner can normally be reached on Monday - Friday 8:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on (703) 308-1323. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or

proceeding should be directed to the receptionist whose telephone number is (703) 308-

1782.

Magid Y Dimyan
Examiner
Art Unit 2825

myd
August 18, 2003

VUTHE SIEK
PRIMARY EXAMINER